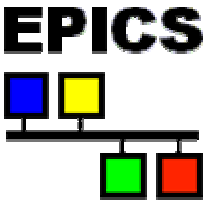
Timing System Development Plans



10 October 2010

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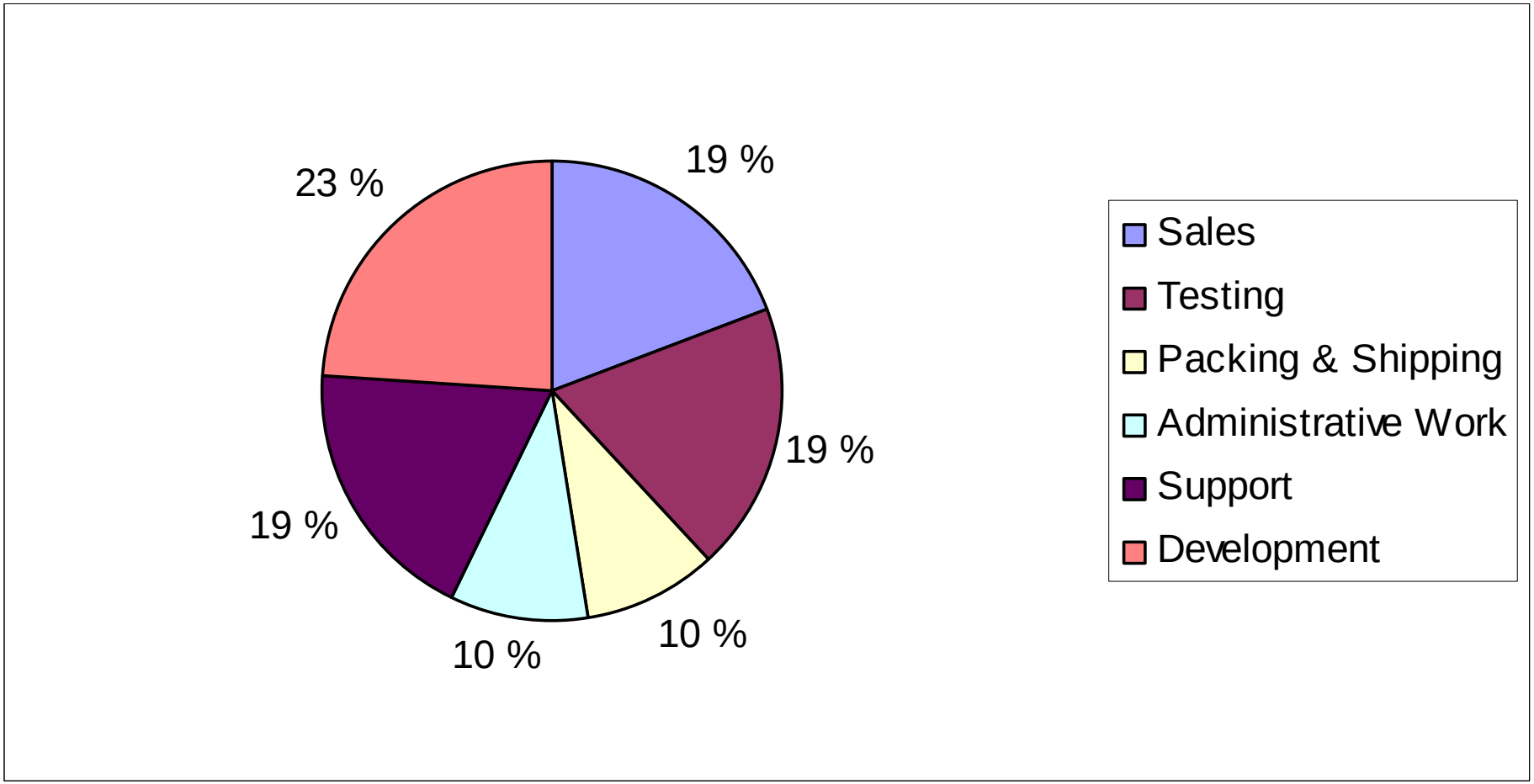
Current Workload



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Motivation for Change

- Not enough time for R&D
- Too much time wasted with software updates (downloading, restarting, ...)
  - Tools run on different linuxes and Windows versions
- Lots of support requests hanging around
- Delays in correspondence
- Insufficient documentation/examples which leads to more support questions
- Web pages out of date

➢ Too much work for one person!

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Options to solve resource issues

- Enlarging Business locally in Finland:
  - Temporarily increase workload
    - Human resources
    - Training
    - Mentoring
  - Decrease level of freedom (currently I'm working > 60% of time from home)

  ► **Not an option**
- Cooperation/Partneship with another Company

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Cosylab

- Cosylab's work with MRF products:
  - PXI firmware additions to CompactPCI EVG/EVR
  - LabVIEW driver support for CompactPCI/PXI EVG/EVR (Joze's MedAustron talk later today)

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Cooperation with Cosylab

- Main Goals
  - Better response to customers' needs
  - Improve level of support/documentation
    - Software support / turn-key solutions
  - Reduce risk of MRF ceasing operation
  - New/better products
- Possibilities
  - Enlarge customer base:
    - Industry could benefit from precise timing

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Cooperation with Cosylab

- Responsibilities
  - MRF will:
    - Focus on R&D
    - Continue with product support
  - Cosylab will:
    - Provide timing solutions / system integration
    - Produce and sell timing system products globally

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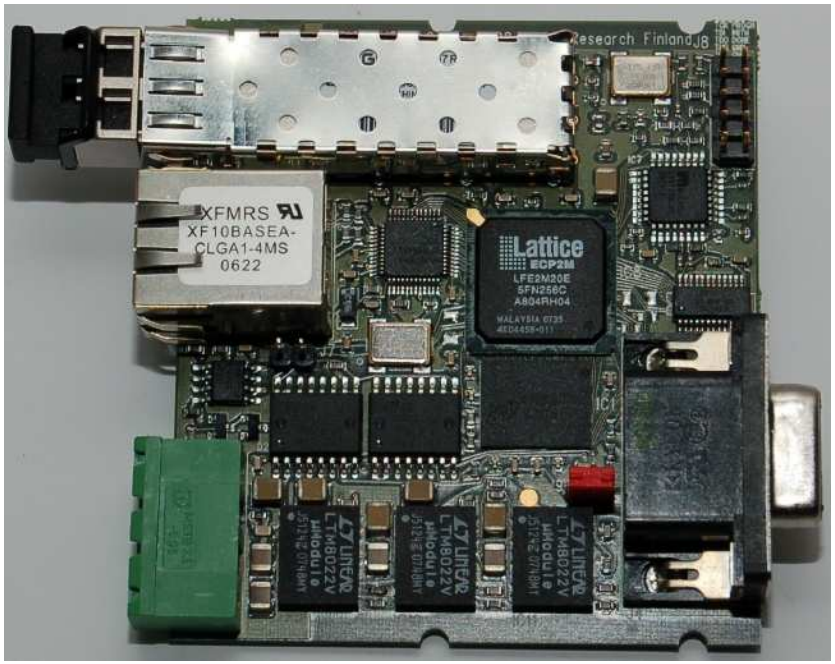
CompactRIO EVR HW

- SFP transceiver for event link
- Lattice ECP2M-35 FPGA with high speed serial link
- 10/100 ethernet
- 64 Mbytes DDR2 memory
- 2 × 16 Mbits serial flash
  - FPGA configuration
  - Software (e.g. RTEMS)
- EEPROM for
  - CompactRIO compliance
  - Store ethernet MAC address
- 5 to 35 VDC power supply input
- 71 mm x 88 mm x 23 mm
- I/O through DSUB15
- ~30 ps RMS jitter



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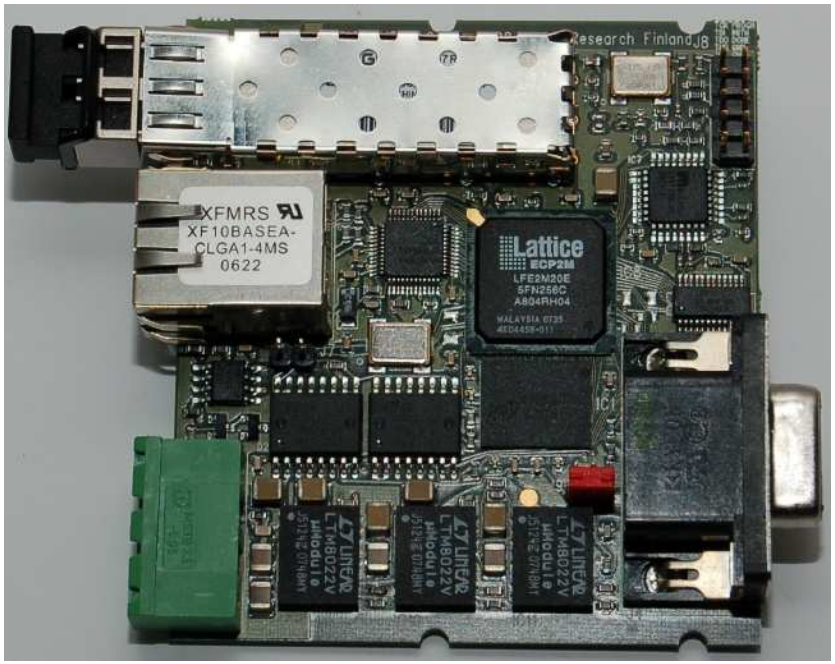
CompactRIO EVR firmware

DSUB15 connections:

- Four programmable outputs (Univ. I/O Outputs in register map)
- Four programmable inputs (Univ. I/O Inputs in register map)
- Configuration through 115200 baud serial interface on two pins (RX & TX)



Challenges (when used with NI HW/LabView)

- Power dissipation ~3W
  - Module has to be placed in slot 1
- Achieve required timing resolution
  - cRIO backplane is running on an internal 40 MHz clock → 25 ns jitter
- Achieve required data transfer capability (serial interface)
- Control and configuration methods
  - cRIO (serial interface)

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CompactRIO EVR further development

- LANS (Doug Gilpatrick and Eric Björklund) have four units
  - Waiting for their comments/suggestions
- Universal I/O carrier board for cRIO EVR with:
  - Two Universal I/O slots
  - USB to serial converter
    - Stand-alone EVR
- EPICS port (RTEMS is already running…)
- Helsinki University is going to use cRIO-EVR for a small carbon isotope accelerator
- Simplified EVG port for cRIO

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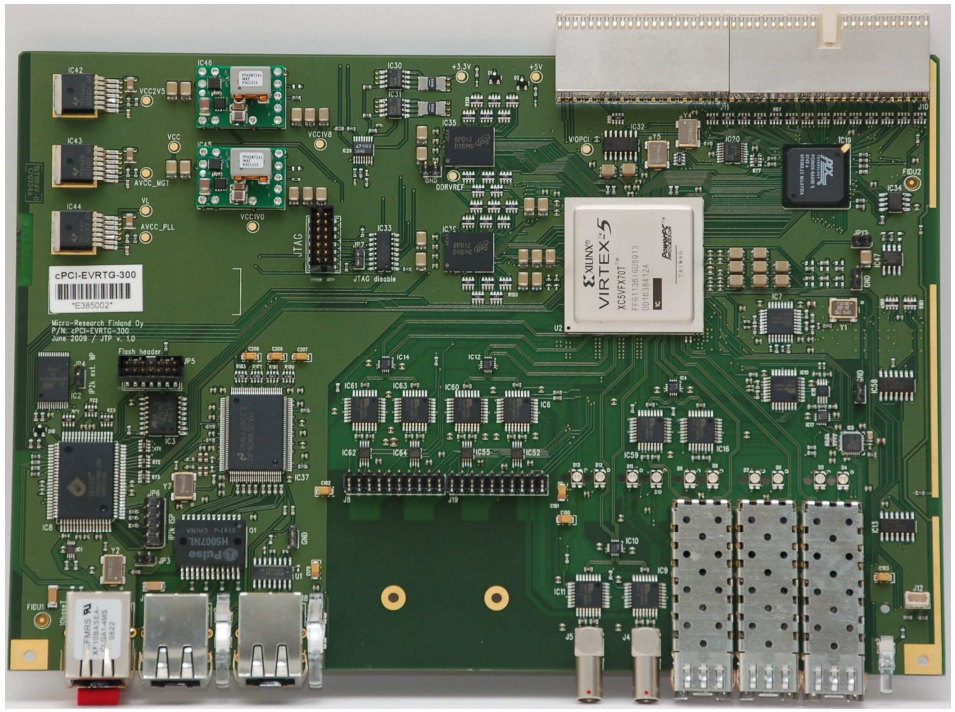
cPCI-EVRTG-300

- 6U form factor CompactPCI
- Based on Virtex 5 FXT
- Eight Outputs:
  - GTX transceiver outputs
  - 40 x event clock resolution
  - Pulse/pattern outputs
  - Frequency generation
  - Two SFPs to drive GUN-RC
  - Two LVPECL outputs
  - Two Universal I/O slots
    - four outputs of choice
    - GUN-TX inhibit input
  - Low jitter (slightly better than VME-EVR-230RF)
  - Delay fine tuning down to ~10 ps steps



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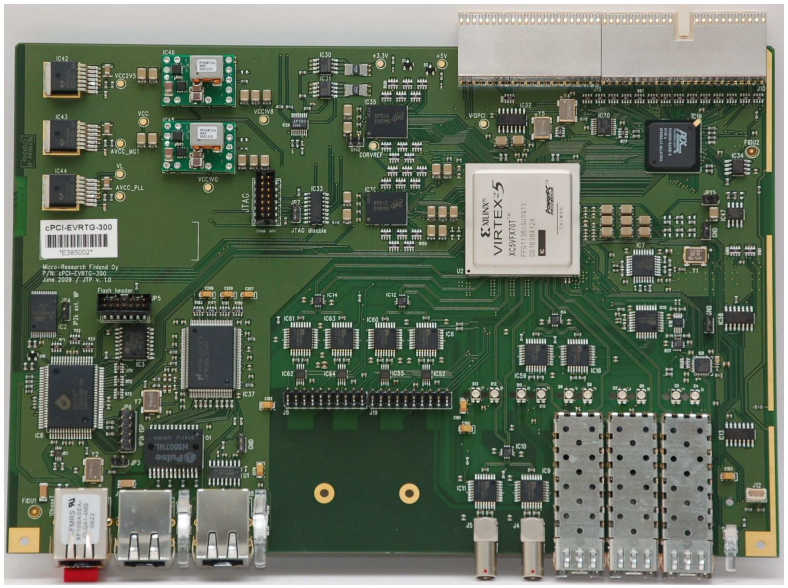
cPCI-EVRTG-300 related development

- New GUN-RC-300 to be designed
- Requirements:
  - One channel
  - Arbitrary pulse patterns with
  - Min. 1 ns pulses
  - Pulse to pulse spacing 2 ns increments
  - Output level 0 to 3.3V
- New modulation scheme
  - 200 ps resolution with GTX
  - > 5 gbps transceivers
  - Modulation decoding and output stage challenging



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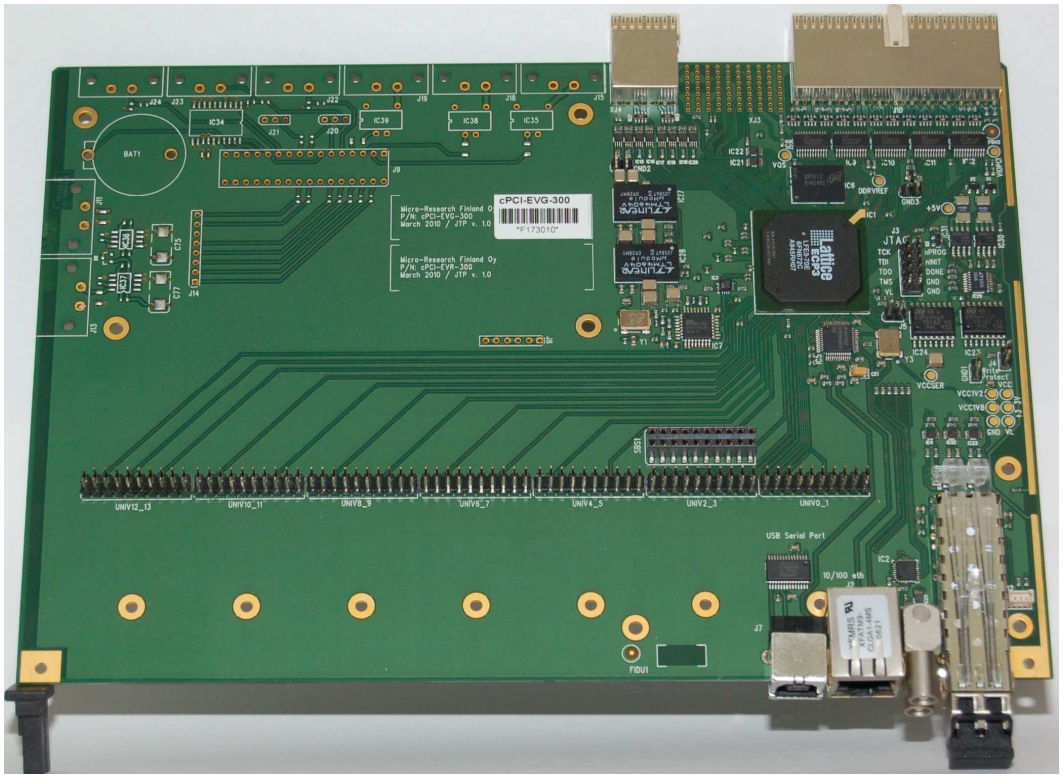
cPCI-EVG-300 and cPCI-EVR-300

- 6U form factor CompactPCI
- Based on Lattice ECP3
- Six Universal I/O slots
- Redesign of cPCI-EVG-230 and cPCI-EVR-230 with same functionality and different form factor
- Target: similar jitter performance as cPCI-EVx-230



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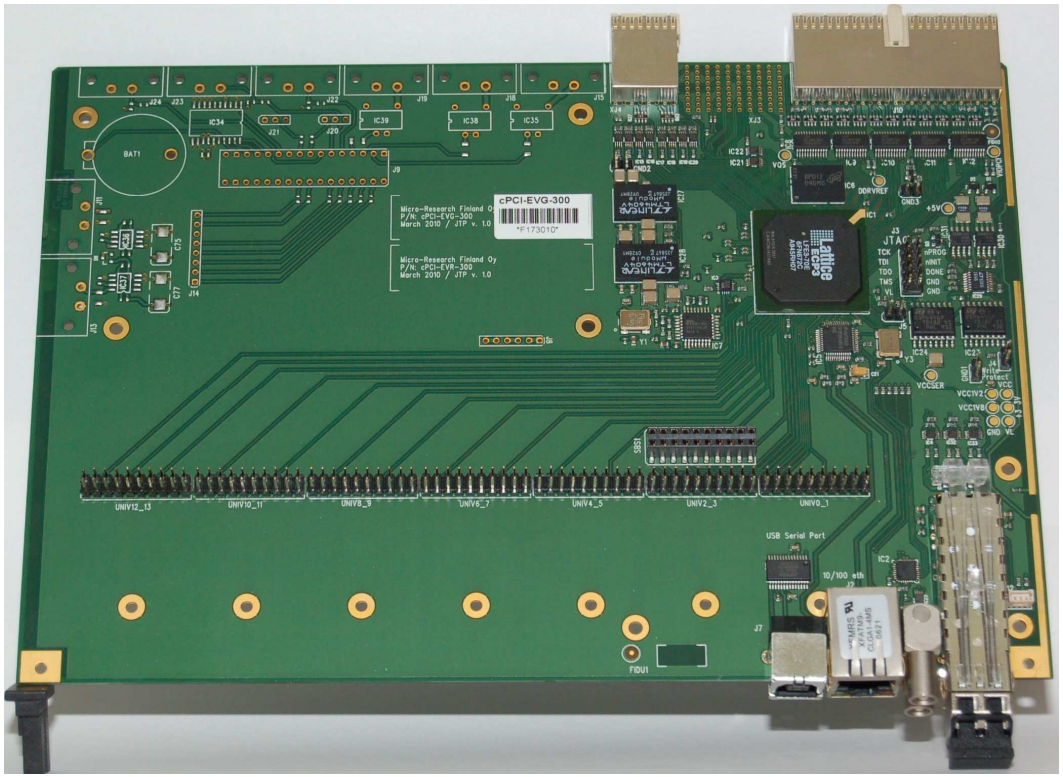
cPCI-EVG-300 and cPCI-EVR-300 further development

- Upgrade to CompactPCI Express
  - Hardware is designed to be able to test this with mounting cPCI Express connector
- 3U version?



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Future Development (wishlist)

- Address all customer requests (firmware issues)
- AMC form factor EVR
  - PICMG/xTCA for Physics
- Timing drift compensation
  - Feasible with current HW
- PCIe form factor EVR?
- Evaluation of new clock cleaners (Silicon Labs, Si5317)
- Data transfer network?

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Future Development (cont.)

- New version (upgrade) of VME-ADC (e.g. for bunch pattern monitoring)
  - Upgrade FPGAs Virtex II Pro to Lattice ECP3?
  - Upgrade ADC? E2V AT84ADC001 (used to be Atmel) to ?

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Modular Register Map

- Modular register map firmware based on one set of source VHDL code
- EVG Versions now available for
  - VME-EVG-230
  - cPCI-EVG-230 (and -220)
  - cPCI-EVG-300
  - (cRIO-EVG)
- EVR Versions now available for
  - VME-EVR-230 & VME-EVR-230RF
  - PMC-EVR-230
  - cPCI-EVR-230 (and -220)
  - cPCI-EVRTG-300
  - cPCI-EVR-300
  - cRIO-EVR

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What's new in Modular Register Map

- SFP transceiver diagnostics
  - RX power, TX power
  - Temperature
- Configuration ROM/RAM
  - Contents not yet specified
- EVG Interrupts
  - Sequencer start/stop interrupts
  - External interrutps
- Pattern CML/GTX outputs
  - Max. 20 x 2048 bit pattern (CML VME-EVR-230RF)
  - Max. 40 x 2048 bit pattern (GTX cPCI-EVRTG-300)
- Frequency outputs (CML/GTX)
  - Define output high/low time in 1/20 (1/40 for GTX) event clocks
  - e.g. Australian Synchrotron booster revolution clock with 217 buckets

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